

Fig.1

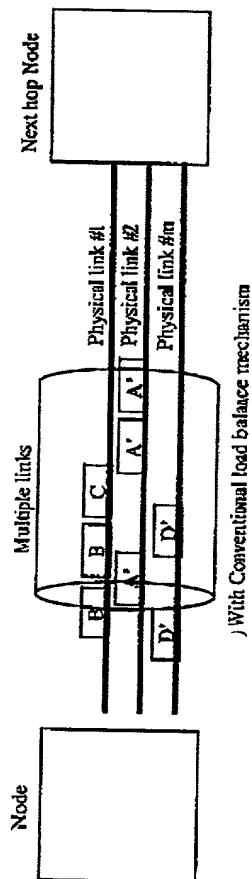


Fig.2

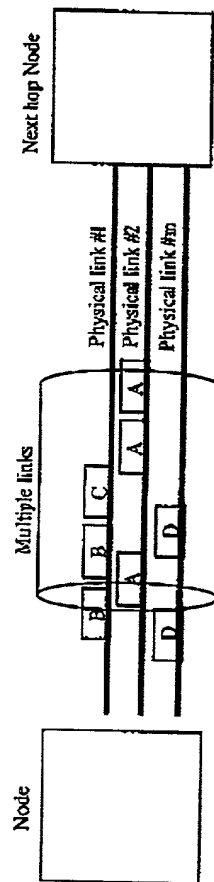
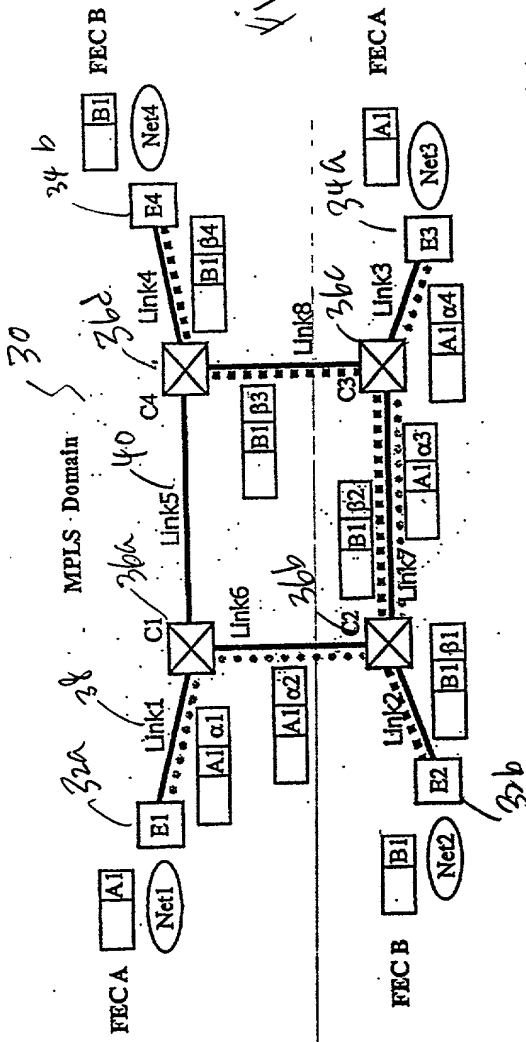


Fig.3



C1, C2, C3, C4 : Label Switch Router (CORE), E1, E2, E3, E4 : Label Switch Router (Edge),
A1, B1: IP Destination Address, α1, α2, α3, α4, β1, β2, β3, β4 : Label

Example of the network (MPLS) domain

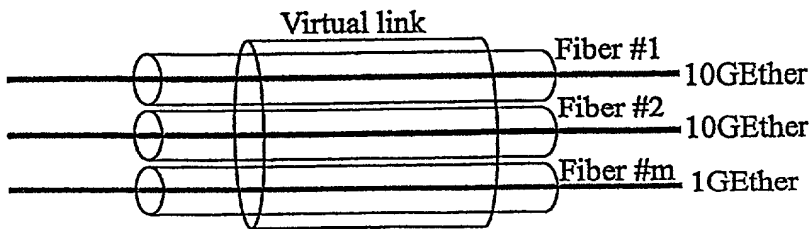


Fig. 5a

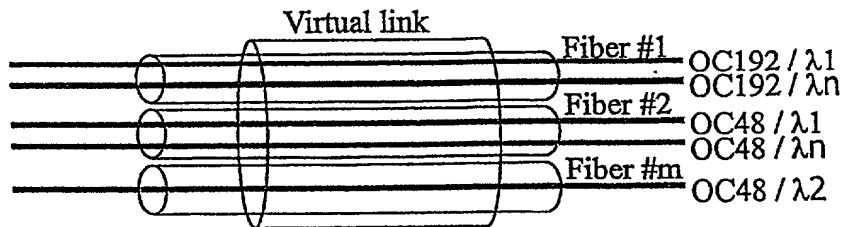


Fig. 5b

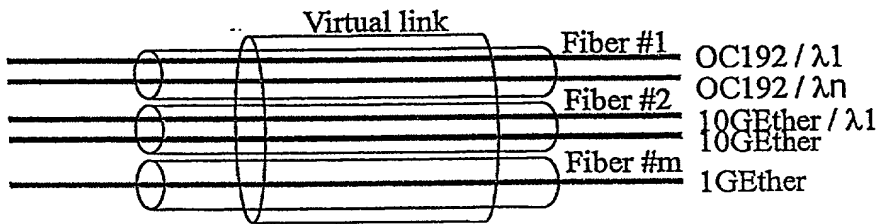


Fig. 5c

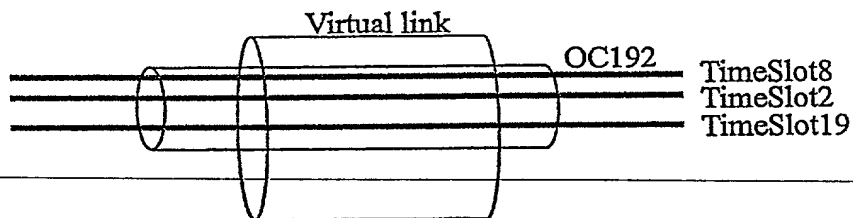


Fig. 5d

Examples of composition of physical and logical links

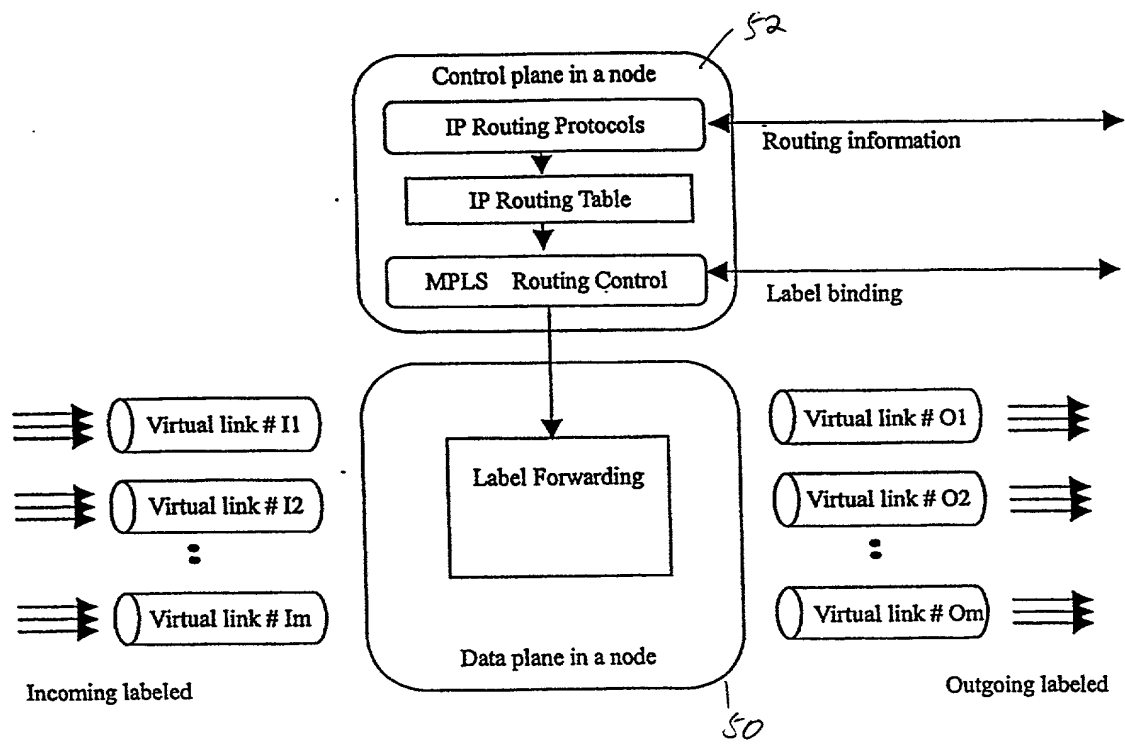


Figure 6 LSR Architecture

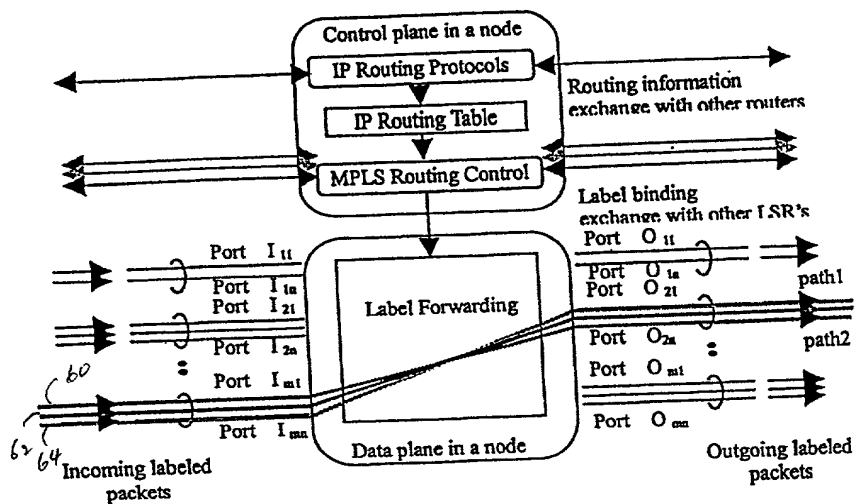


Figure 7

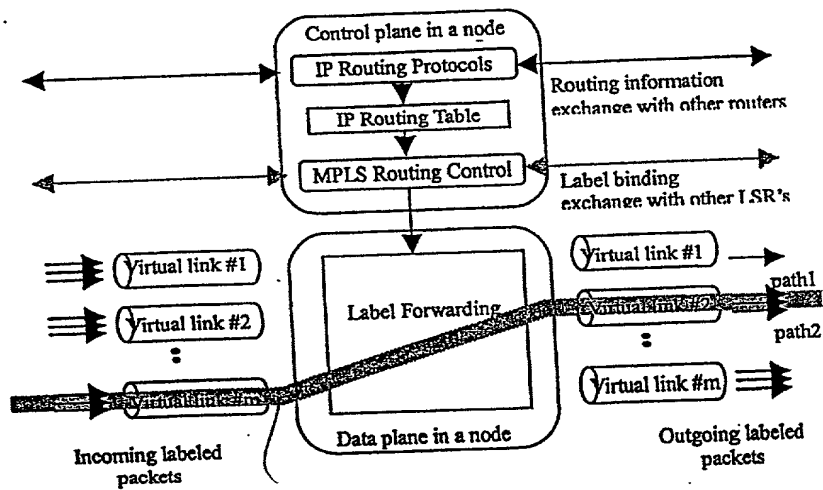


Figure 8

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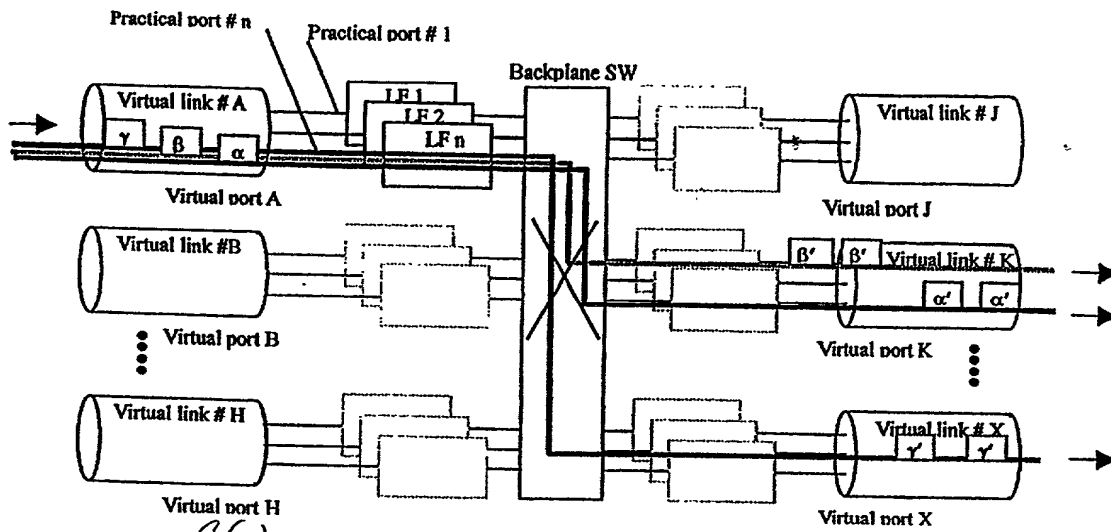


Figure 9(a)

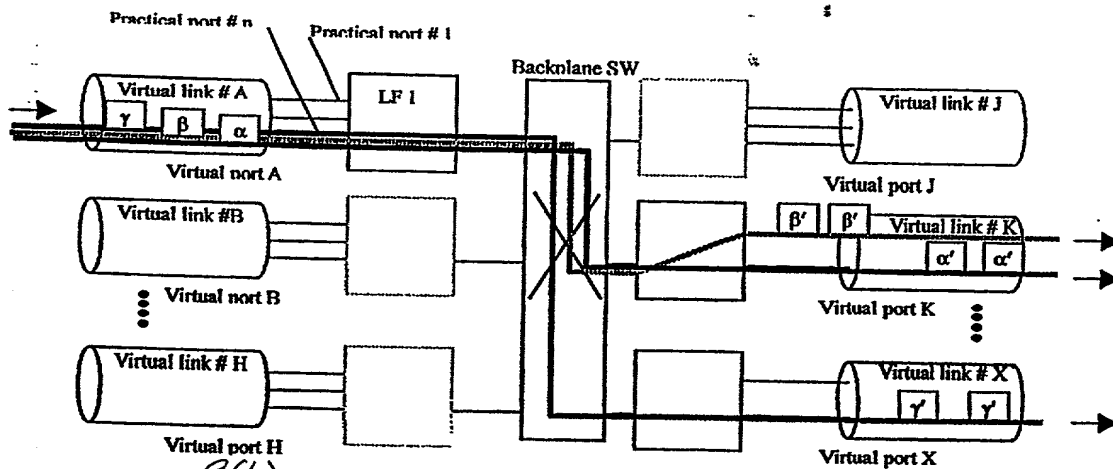


Figure 9(b)

90 92 94 96
Label Forwarding Table maintained by the MPLS control plane

	Input practical port #	Input virtual port #	Input Label	Output Label	Output virtual port #	Output practical port #
	n	A	α	α'	K	$f(\alpha')$
	n	A	β	β'	K	$f(\beta')$
	n	A	γ	γ'	X	$f(\gamma')$
	2	A	δ	δ'	B	$f(\delta')$
	1	A	ϵ	ϵ'	B	$f(\epsilon')$
	2	A	ζ	ζ'	H	$f(\zeta')$
	1	A	η	η'	J	$f(\eta')$
	5	A	σ	σ'	K	$f(\sigma')$
	n	A	κ	κ'	X	$f(\kappa')$

Figure 7 Label Forwarding Table and mechanism to decide practical output port at the sending LSR

98 100 90 92 94 96
Label Forwarding Table maintained by the MPLS control plane

Tag	Hash value of incoming label	Input practical port #	Input virtual port #	Input Label	Output Label	Output virtual port #	Output practical port #
○	$f(\alpha')$	n	A	α'	α''	K	$f(\alpha'')$
○	$f(\beta')$	n	A	β'	β''	K	$f(\beta'')$
○	$f(\gamma')$	n	A	γ'	γ''	X	$f(\gamma'')$
○	$f(\delta')$	2	A	δ'	δ''	B	$f(\delta'')$
○	$f(\epsilon')$	1	A	ϵ'	ϵ''	B	$f(\epsilon'')$
○	$f(\zeta')$	2	A	ζ'	ζ''	H	$f(\zeta'')$
○	$f(\eta')$	1	A	η'	η''	J	$f(\eta'')$
○	$f(\sigma')$	5	A	σ'	σ''	K	$f(\sigma'')$
○	$f(\kappa')$	n	A	κ'	κ''	X	$f(\kappa'')$

Figure 8 Fast lookup mechanism using a hash